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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/920,275	07/31/2001	Gregory M. Chrysler	042390.P12135	5708

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EXAMINER

GEYER, SCOTT B

ART UNIT PAPER NUMBER

2829

DATE MAILED: 04/24/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/920,275

Applicant(s)

CHRYSLER ET AL

Examiner

Scott B. Geyer

Art Unit

2829

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on 10 April 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☐ Claim(s) 8-17, 25 and 27 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) 8-11 is/are allowed.
- 6) ☐ Claim(s) 12-17, 25 and 27 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on 21 July 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 9.
- 4) ☐ Interview Summary (PTO-413) Paper No(s) _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other

DETAILED ACTION

1. The indication of allowable subject matter of claim 26 has been withdrawn in light of the newly supplied references in the IDS, paper no. 9. The examiner notes that claim 25 has been amended by the applicant to include the subject matter of claim 26, and claim 26 was cancelled. Claims 25 and 27 are treated on their merits below.

Information Disclosure Statement

2. The references cited within the information disclosure statement, entered as paper no. 10, have been considered.

Claim Objections

3. Claim 13 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. Claim 13 recites only the limitations that were already recited in claim 12. Claim 13 has not been treated further on its merits since claim 12 has been fully rejected below on its merits. Claims 14 and 15 are also objected to as being dependent upon an objected claim.

Claim Rejections - 35 USC § 112

4. Claim 15 as amended by the applicant is acceptable and the rejection of claim 15 under 35 USC 112, 2nd paragraph has been withdrawn.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 12, 14 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pollock et al. (EP 0 814 5098 A2) in view of Wolf et al. (Silicon Processing For The VLSI Era, Volume 1).

7. As to **claim 12**, Pollock et al. teach in figure 2: a layer of solid diamond (12) having an exposed lower surface, a layer of semiconductor material (14) on the diamond layer and an integrated circuit (21) on the side of the semiconductor material opposite the layer of diamond. Pollock et al. further teach attachment of the diamond layer to the semiconductor layer before individual die are cut (see column 2, lines 48 et seq.). Cutting of the die would provide singulated die. Pollock et al. does not specifically teach monocrystalline semiconductor material. However, Wolf et al. teach single crystal (monocrystalline) silicon used to make silicon wafers for integrated circuits (page 1-8). Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the device of Pollock et al. with monocrystalline

silicon as taught by Wolf et al. Monocrystalline silicon is preferred for semiconductor devices over polycrystalline silicon since polycrystalline silicon exhibits too many crystal imperfections which translates into short minority carrier lifetimes.

8. As to **claim 14**, Wolf et al. teach a monocrystalline semiconductor material as stated above and both Wolf et al. and Pollock et al. teach silicon as a semiconductor material.

9. As to **claim 17**, Pollock et al. teach a die having a rectangular outline when viewed from above (see figure 2).

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10. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Pollock et al. (EP 0 814 5098 A2) and Wolf et al. (Silicon Processing For The VLSI Era, Volume 1) as applied to claim 14 above, and further in view of Schrantz et al. (WO 94/15359).

11. As to **claim 15**, Pollock et al. and Wolf et al. teach all the limitations except for a layer of polysilicon between the layer of monocrystalline silicon and the layer of solid diamond. However, Schrantz et al. teach, in figure 3, a layer of polysilicon (16) between a layer of diamond (12) and a crystalline silicon wafer (18). It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the device of Pollock et al. and Wolf et al. with a layer of polysilicon between a layer of diamond and a silicon wafer to ensure a reliable bond between the silicon wafer and the diamond layer.

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12. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Pollock et al. (EP 0 814 5098 A2) and Wolf et al. (Silicon Processing For The VLSI Era, Volume 1) as applied to claim 12 above, and further in view of official notice.

13. As to **claim 16**, Pollock et al. and Wolf et al. teach all the limitations except for the plurality of contacts on the integrated circuit. Official notice is taken that it is well known in the art of semiconductor devices that integrated circuits have a plurality of contacts. It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the device of Pollock et al. and Wolf et al. with a plurality of contacts so as to provide a means for electrically connecting the integrated circuit to a substrate such as a motherboard.

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14. Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Pollock et al. (EP 0 814 5098 A2) in view of Tanabe et al. (6,051,063), Wolf et al. (Silicon Processing For The VLSI Era, Volume 1) and official notice.

15. As to **claim 25**, Pollock et al. teach in figure 2: a layer of solid diamond (12), a layer of semiconductor material (14) on the diamond layer and an integrated circuit (21) on the side of the semiconductor material opposite the layer of diamond. Pollock et al. further teach the diamond film having a thickness of 10-20 mils (254-508 microns) (see column 3, lines 46-48). Pollock et al. also teach formation of a plurality of electronic devices on the entire substrate structure, which is graphically represented by numeral 21 in figures 1 and 2 (see column 3, lines 35-41). Pollock et al. does not

specifically teach a diamond layer having a thickness less than 150 microns, a monocrystalline semiconductor material, or a plurality of integrated circuits in rows and columns. However, Tanabe et al. teach a diamond film utilized in a similar integrated circuit device, wherein the diamond film has a thickness less than 150 microns. Wolf et al. teach single crystal (monocrystalline) silicon used to make silicon wafers for integrated circuits (page 1-8). Official notice is taken that it is well known in the art of semiconductor devices that a plurality of devices would be formed on a wafer surface in a pattern of rows and columns. It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the device of Pollock et al. with a diamond film having a thickness less than 150 microns as taught by Tanabe et al. so as to provide a thinner, and thus smaller and more lightweight semiconductor package. Also, it would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the device of Pollock et al. with monocrystalline silicon as taught by Wolf et al. as monocrystalline silicon is preferred for semiconductor devices over polycrystalline silicon since polycrystalline silicon exhibits too many crystal imperfections which translates into short minority carrier lifetimes. Finally, it would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the device of Pollock et al. with a plurality of integrated circuits in rows and columns to facilitate ease in separation with a dicing saw at the time when the individual dies would be needing separation from the wafer for further packaging.

16. As to **claim 27**, Wolf et al. teach a monocrystalline semiconductor material as stated in paragraph 15 above, and both Wolf et al. and Pollock et al. teach silicon as a semiconductor material.

Allowable Subject Matter

17. Claims 8-11 are allowed.

18. The following is a statement of reasons for the indication of allowable subject matter: claims 8-11 were indicated as allowable in the previous office action, entered as paper no. 7.

Response to Arguments

19. Applicant's arguments with respect to claims 12-17, 25 and 27 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

20. Applicant's submission of an information disclosure statement under 37 CFR 1.97(c) with the fee set forth in 37 CFR 1.17(p) on 4-10-03 prompted the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 609(B)(2)(i). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

21. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Scott B. Geyer whose telephone number is (703) 306-5866. The examiner can normally be reached on weekdays, between 10:00am - 6:30pm. The examiner may also be reached via e-mail: scottt.geyer@uspto.gov

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on (703) 308-1233. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9318 for regular communications and (703) 872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

SCOTT GEYER
PATENT EXAMINER

SBG
April 17, 2003

